

THE SILICON SENSOR FOR THE COMPACT MUON SOLENOID – CONTROL OF THE FABRICATION PROCESS

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Abstract. The Compact Muon Solenoid (CMS) is one of the experiments at the Large Hadron Collider (LHC) under construction at CERN. The inner tracking system of this experiment consist of the world largest Silicon Strip Tracker (SST). In total 24244 silicon sensors are implemented covering an area of 206 m². To construct this large system and to ensure its functionality for the full lifetime of ten years under the hard LHC condition, a detailed quality assurance program has been developed. This paper describes the strategy of the Process Qualification Control (PQC) to monitor the stability of the fabrication process throughout the production phase and the results obtained are shown.

Key words: CMS Silicon Strip Tracker

1. INTRODUCTION

The Compact Moon Solenoid (CMS) [1] aims at cleanly detecting the different signatures of new physics at LHC (Large Hadrons Collier) by identifying and precisely measuring electrons, moons photons and jets over a large energy range. This experiment will observe pp collision at 14 Ted of center-of-mass energy with a luminosity of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and with the bunch crossing frequency of $1/25\text{ns} = 40 \text{ MHz}$.

The core of the apparatus is a superconducting solenoid, which generates a 4T magnetic field and contains a central tracking system together an electromagnetic and hadron calorimeter. The tracker measurements are combined with track segments reconstructed in the outer muon system to extend the kinematic region of a precise muon momentum measurement. The physics requirements for the CMS Tracker performance are a momentum resolution of $\sim 1\text{-}2\%P_T$ at $\sim 100 \text{ GeV}/c$, an impact parameter resolution of 35 μm in the transverse plane and of 75 μm in the longitudinal direction [2], [3].

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The CMS tracking system is fully based on silicon detector technology [2], [5]. One of the critical issues of the Silicon Strip Tracker (SST) is the long-term survival after heavy irradiation.

The system has to be designed to guarantee stable operating conditions for about 10 years of LHC running. In this period the most irradiated detector of SST will be subjected to an average fluence of $1.6 \times 10^{14} \text{ 1-MeV- equivalent neutrons/cm}^2$.

1. TRACKER LAYOUT

The natural coordinate frame used to describe the CMS detector geometry is a right-handed system with the x -axis pointing to the centre of the LHC ring, the z -axis coincident with the CMS cylinder axis and the y axis directed upward along the vertical. The cylindrical symmetry of CMS design drives to use a pseudo-angular reference frame given by r , the distance from the z -axis, Φ , the azimuthal coordinate with respect to the x -axis, and η , the pseudo-rapidity.

The CMS tracker consists of ten barrel layers, plus two sets of nine endcap disks, altogether covering a pseudorapidity range of $|\eta| \leq 2.5$. The layout is shown in Fig. 1. Four inner barrel layers (TIB) are assembled in shells complemented by two inner endcaps each composed of three small disks (TID). The outer barrel structure (TOB) consists of six concentric layers closing the tracker towards the calorimeter. The endcap modules (TEC) are mounted in seven rings on nine disks per each side consisting of sectors.

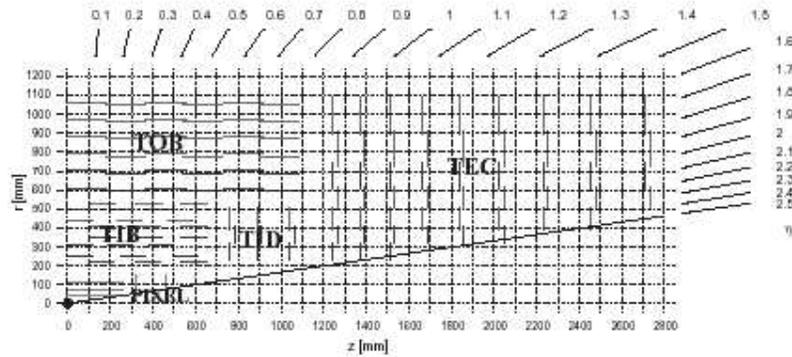


Fig.1 – Sketch of the tracker layout – one quarter longitudinal view

A pixel vertex detector will be mounted further inside of the silicon strip detector.

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The complete tracking volume will rest in an inert Nitrogen atmosphere at -10°C to avoid the effects of reverse annealing.

2. SILICON STRIP DETECTOR DESCRIPTION

The SST is equipped with 24244 single-side micro-strip sensors manufactured using $6''$ technology, with the standard planar process, covering an active area of 206 m^2 . The main strategies of CMS to ensure the radiation hardness

of the silicon sensors consist of reducing the surface damage, delaying the bulk type inversion and using stable sensors with respect to high voltage. One single detector is produced from each wafer and the crystal lattice orientation is of $\langle 100 \rangle$ type [6].

The wafer thickness is required to be 320 μm for “thin” sensors, with a substrate resistivity in the range 1.5÷3,25 $\text{K}\Omega\text{cm}$, and 500 μm for “thick” sensors, with a request resistivity of 4÷8 $\text{K}\Omega\text{cm}$. A typical silicon detector is based on n-type bulk material in which a p^+ implantation is used on the front side to define the strip-shaped diode. Once the junction is under reverse bias voltage, all free carriers in the bulk are drained by the electric field. On top of each strip an integrated capacitor is built for signal read-out.

An array of poly-silicon resistors, with a resistance value requested to be 1.5 ÷ 0.5 $\text{M}\Omega$, is used to bias the implanted strips. The resistors connect the bias ring to the corresponding p^+ - implant of the strip through a metallized probe pad (DC pad). Two rows of AC pads are used at the ends of the strips to allow for bonding and testing.

A schematic view of the detector active region is shown in Fig. 2.

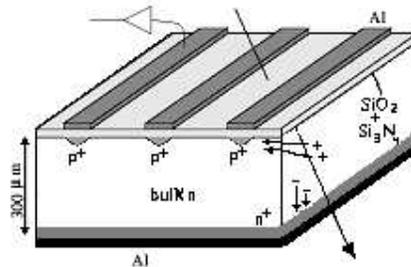


Fig. 2 – A schematic view of a detector.

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On the sensor backside, providing an ohmic contact between the bulk and the metal layer, a uniformly metallized n^+ layer is implanted. The presence of this highly doped n^+ layer acts as a barrier for minority carriers coming from the depleted bulk.

3. CONTROL OF THE FABRICATION PROCESS

4.1 The test structure

The Process Quality Control (PQC) aims to monitor the stability of the sensor fabrication process throughout the production and to identify any problem as soon as possible. For this reasons, the wafer hosts additional devices beyond the main detector. The percentage of wafers tested is 5% of the total number and at least one wafer per sensor batch is analyzed.

A standard set of nine structures, called half-moon, is placed inside the fiducial region and it is shown in Fig.3.

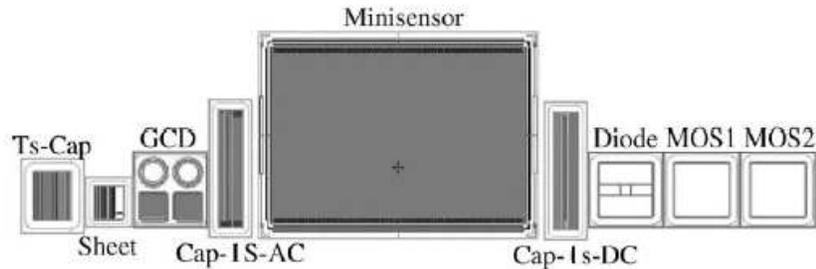


Fig.3 – The standard test structure.

The design is identical for all sensor geometries and from left to right it is composed of:

- Ts-Cap, a device used to analyse the quality of the dielectric, measuring its breakdown voltage and the capacitance value. This device is an array of 26 AC coupled strips characterized by the same dielectric composition of the main sensor but with a direct connection to the bias ring, without polysilicon resistors.
- Sheet, a device composed by nine superficial structures, used to measure sheet resistance: three implant strips, three aluminum strips, three polysilicon resistors, all lying directly on the n-doped bulk.

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- GCD, used to study the quality of the silicon-oxide interface through the measurement of the surface current. This structure hosts a square Gate Controlled Diode (GCD) and it is composed by a comb shaped MOS intertwined with a comb made of p⁺ implanted strips.
- Cap-IS-AC (Inter-strip Capacitance AC) is a device built of a set of nine strips with the same structure of the main sensor. This structure is used to measure the inter-strip capacitance between the central strip in the group of nine, and the two neighboring ones. The three external strips on each side are connected together their metallization, to stimulate the effect on the capacitance of the strips beyond the first neighbors, in order to minimize the number of connections.
- The mini-sensor, is a small-size replica of the main sensor. It is a rectangular detector, composed by 192 strips at a pitch of 120 μm. This value is an average among the pitches of the different sensor geometries characterizing the SST. A second row of pads is displaced by 2 mm with respect to the bias-ring, in order to perform bonding tests.
- Cap-IS-DC (Inter-strip Capacitance DC) is aimed to measure the inter-strip resistance. This device has a similar structure to Cap-IS-AC, except for the fact that the strips are not connected to the bias ring, either directly or

through a bias resistor. In addition, the capacitor dielectric layer is missing in the strips and the p^+ implant can be contacted all over their length.

- Diode, a simple square diode, of area 0.24 cm^2 , surrounded by a guard ring is designed to measure the depletion voltage.
- The MOS device is designed to measure the oxide thickness and the flat band voltage value. This structure with the dielectric composition corresponding to the thick oxide layer present in the inter-strip region of the main detector has a gate area of 0.24 cm^2 .

4.2 The instrumental set-up

The Process Qualification tests are performed in three laboratories, Florence, Strasbourg and Vienna, in the controlled environment of the clean room. The three centers have similar equipment and this has allowed us to develop a common set-up for the measurements. The schematic of the common set-up is shown in Fig. 4.

The standard test structure is placed in a probe-station where all the nine structures are contacted by a probe card produced by Mesatronic (France) in collaboration with the PQC laboratories.

The 40 channels of the probe-card are connected via a Keithley 7002 switching matrix system to the measuring instruments.

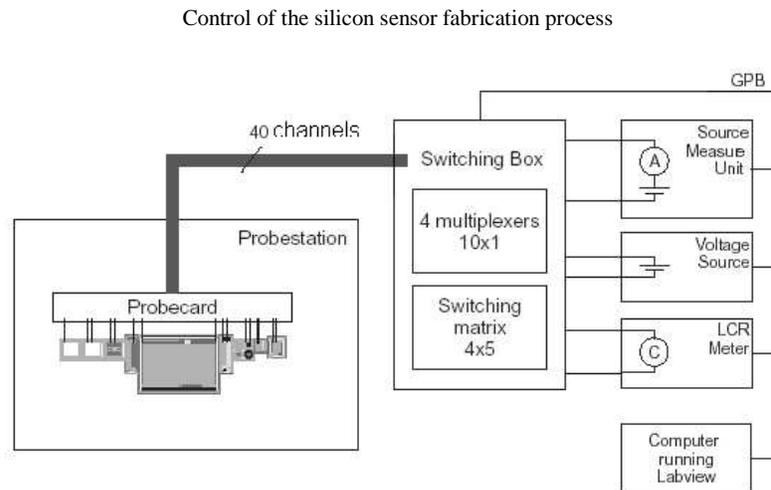


Fig.4 – Schematic of the common instrumental set-up.

This system hosts a first multiplexing layer of four 10x1 K7154 modules and a second layer built of 4x5 K7153 module. The nine measurements require a DC voltage source that supplies at least 700 V, a second voltage source up to 20 V, a pico-amperometer and a capacimeter. A PC running a National Instrument Labview software via the GPIB protocol controls all the instrumentation.

The acquisition software, performing in an automatic run, has three components: acquisition, analysis and database interface. When is necessary, the software analyses and fit the data to extract the relevant PQC parameters. This is the case for CV on MOS, CV on diode and IV on gate controlled diode. The basic tool for the analysis is the linear fit, which is used to find kinks between different linear regions. At the end for each measurement a flag is set to indicate the positive or negative outcome of the test. The results are summarized in a XML file, ready to be inserted in the CMS Tracker construction database.

4. RESULTS OBTAINED BY THE PQC

In this section a selection of the results obtained with the test structure corresponding of the sensor batches delivered so far is presented. At the time of this report the number of wafers that have been tested in the PQC is around 3840.

An important parameter monitored by the PQC regard the resistivity of the aluminum.

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The resistance of the aluminum layer deposited on top of the strips is a parameter that contributes to the input noise seen by the front-end electronics.

This measurement is performed on the device called sheet which consist of nine sheet structures used to measure the resistivity of the aluminum layer, of the p⁺ implant and of the polysilicon resistors. All nine structures have individual contacts at the bottom of the device, whereas the other side is connected to the common bias ring. The resistivity of the aluminum is estimated with the first set of three strips, containing 50, 20 and 10 μm wide strips of the same length. The measured resistance scales with the length and the inverse of the width.

The specific resistivity ρ/sq. in [Ω/sq.] can be calculated using the equation 1, knowing the ratio of width to length w/l and the contact resistance of the measurement set-up R₀.

$$\rho / \text{sq.} = (R - R_0) \cdot w / l \quad (1)$$

At the beginning of production the surface resistivity was exceeding our specifications ($\rho_{Al} < 30 \text{ m } \Omega \text{ square}$). This problem has been solved with an increase in the aluminum implant depth from 1.2 to 2.0 μm. The results obtained are shown in Fig. 5.

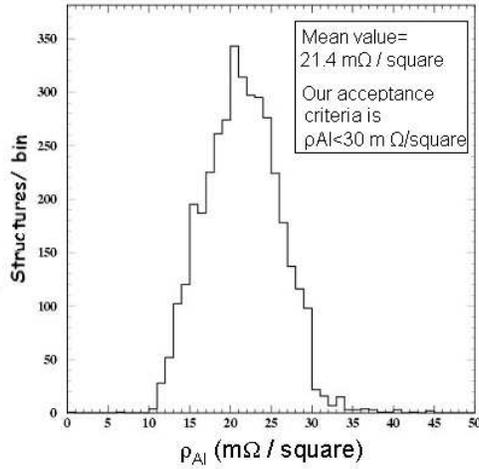


Fig.5 – Distribution of the aluminum resistivity measured on 3840 test structures.

Other important parameters monitored by PQC regard the depletion voltage and the wafer bulk resistivity. The CMS Tracker request to have a depletion voltage below 400 V after 10 LHC years leads to the following requirements on the bulk resistivity measured through a CV curve at 100 KHz on the diode: $1.25 < \rho < 3.25$ KΩ per cm in the inner tracker and $4.5 < \rho < 7.5$ KΩ per cm in the outer tracker.

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The silicon bulk is biased by a voltage varied between 0 and 300 V, where the capacitance is measured at steps of 5 V. Two linear fits are applied to the $1/C^2$ curve as a function of the applied voltage. The depletion voltage corresponds to the intersection of the two linear regions (see Fig. 6).

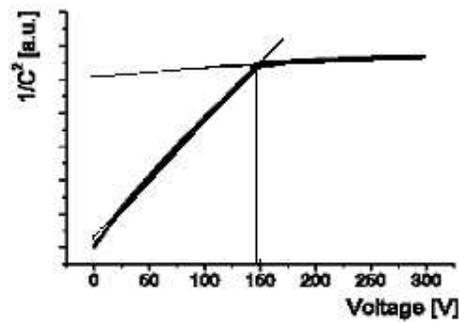


Fig.6 – The function $1/C^2$ (V) with linear fits to determine the depletion voltage.

The results obtained are shown in Fig. 7.

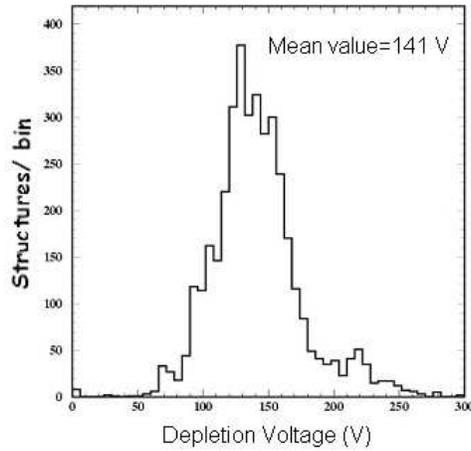


Fig.7. – Distribution of the depletion voltage measured on 3840 test structures.

Because of geometrical reasons, the depletion voltage measured with these structures differs to a sensor with the same size but segmented strips [7]. Thus, comparing the depletion voltages of the sensor and the test structure, one has to take this geometric factor into account (approx. $V_{\text{depl (Sensor)}} \approx 1.35 \cdot V_{\text{depl (Diode)}}$) for the sensors used in the inner tracker (IB2) (see Fig 8).

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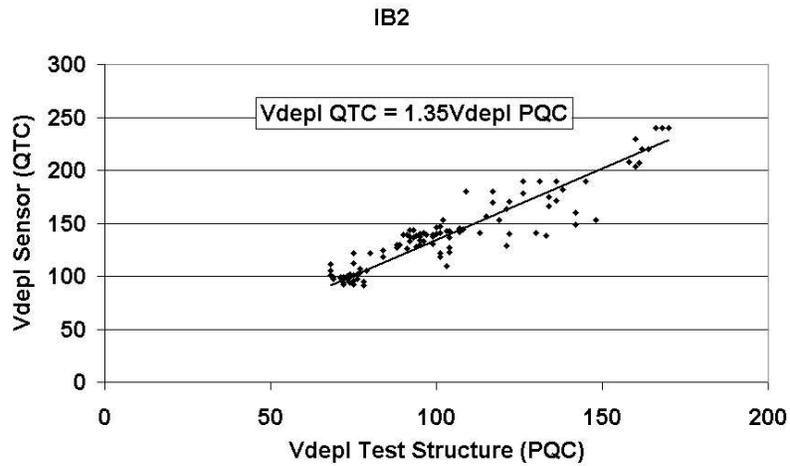


Fig. 8 – The difference between the depletion voltages measured on the sensor and on the test structure (IB2 geometries)

A problem is detected, after the PQC has verified the failure of some sensor batches to satisfy the resistivity condition the company has agreed to substitute the problematic batches.

6. CONCLUSIONS

The proton – proton collisions inside the CMS apparatus will create an enormous radiation background, which will damage every detector material. The innermost layers of the silicon strip detector will receive an estimated fluence of 1.6×10^{14} neutrons cm^{-2} (1 MeV neutron equivalent) during 10 years of LHC operation. The fluence is gradually lower for the sensors mounted further away from the interaction point. The two most important macroscopic effects of the irradiation are the increase of the leakage current which is linear with fluence, and the conversion of the n-type bulk into p-type with ever-increasing bias voltage after type inversion, which eventually leads to detector break-down.

An appropriate choice of the resistivity of the original silicon wafers is important to influence the evolution of the depletion voltage. CMS Collaboration has decided to use different material for the inner part of the tracker compared to the outer part.

The low resistivity sensors for the inner part of the detector will require a high bias voltage at startup (up to 330 V), however the type inversion will occur at a higher fluence and hence later in time. At the end of the foreseen lifetime of 10 years, the

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sensors, which are exposed to the highest fluence, will require a bias voltage, which is not much higher than the one at startup. For the sensors in the outer part the choice of high resistivity material allows the use of thicker wafers with still manageable depletion voltage.

To monitor all important electrical parameters, which contribute to obtaining the best performances of the silicon strip detectors and the stability of its production, an elaborate working system has been developed and it was presented in this paper. Except for the above mentioned problems, we found that the monitored parameters show good fabrication process stability in time.

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