

FREQUENCY MEASUREMENT OF A PULSED RF OSCILLATOR

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Abstract. A method to measure the frequency of a pulsed RF oscillator, based on the phase-locked loop principle is described. An analog sample and hold circuit synchronized by the gate signal is used to store the error voltage for VCO during the pauses between RF pulses.

Key words: superregenerative oscillator, frequency measurement, phase-locked loop circuit.

A simple method for the frequency measurement of a pulsed RF oscillator is described. This method has been developed, especially, in order to perform an accurate frequency monitoring of a superregenerative oscillator (SRO). Although the basic principles of SRO are early discovered and well known [1, 2] it is still widely used in the study of the RF absorption energy by various physical systems, in low cost RF and microwave applications and, recently, included in ultra wide band (UWB) communication systems [3–5]. Generally, the output signal of a SRO consists of a RF pulses train. The amplitude demodulated RF signal provided by a SRO, called quenching signal, is used to detect RF absorption. The study of the RF absorption due to various physical effects (*e.g.* cyclotron resonance, nuclear resonance, parametric resonance of the stored ions, RFSE effect, etc.) requires measuring the precise frequency where the RF absorption occurs. On the other hand, a SRO is characterized by poor frequency stability. As a consequence a continuous control of the SRO operating frequency is required. The use of a spectrum analyzer is not always possible because the frequency spectrum of a SRO contains a lot of discrete frequencies (sidebands) so that it is not easily to distinguish the fundamental line. Taking into account characteristics of the SRO signal above mentioned, to measure the carrier frequency of a SRO is equivalent to measure the frequency of a pulsed RF oscillator.

The system described in this paper is based on the PLL (phase-locked loop) principle. The block diagram of a conventional PLL system is presented in Fig. 1.

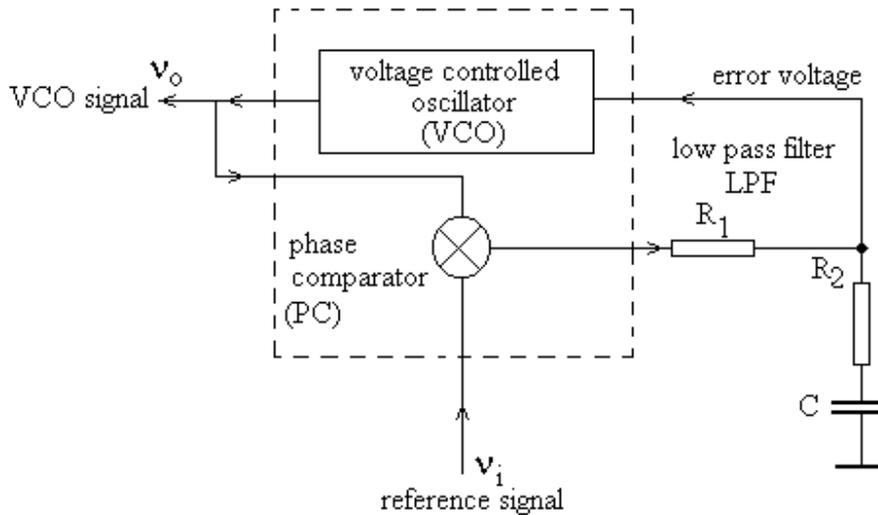


Fig. 1 – The conventional topology of a PLL circuit.

To the two inputs of a phase comparator (PC) is applied an external signal (called reference signal) and a signal yielded by a voltage controlled oscillator (VCO), respectively. The signal provided at the output of the phase comparator filtered by a low pass filter (LPF) is called error voltage and serves as control voltage for the VCO. The frequency of the output signal of a VCO varies linear as a function of the voltage applied to its control input. The system is designed to act so that VCO signal keeps a constant phase angle relative to the reference signal. In this way a PLL circuit operates as a negative feedback system. When the PLL circuit is in the “locked” condition, the reference signal frequency v_i is equal to the VCO frequency v_o [6].

A method aimed to measure the frequency of a pulsed RF oscillator has been developed based on PLL principle above described. In this purpose a modified PLL circuit topology is used. The modified topology is shown in Fig. 2. As an input (reference) signal is used the pulsed RF signal (RF signal provided by SRO). The RF amplitude demodulated signal or quenching signal is used as a gate signal. The feedback loop is interrupted by an analog switch (AS). The analog switch isolates the output of the phase comparator from the control input of the VCO during the pauses between RF pulses. The quenching signal controls the state of the analog switch; on or off. The operational amplifier operating as a voltage repeater, due to its high input impedance prevents discharge of the capacitor C. The analog switch is controlled so that it is off during the pauses between RF pulses. In this purpose the quenching signal must be correct phased. Thus, the analog switch (AS), low pass filter (LPF) and operational amplifier acts as a sample and hold circuit storing the error voltage for VCO during the pauses between RF pulses.

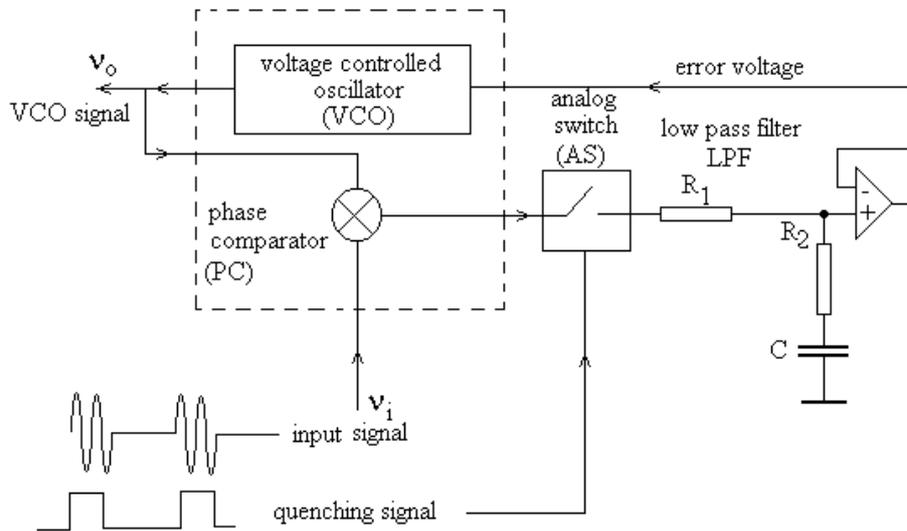


Fig. 2 – Modified topology of a PLL circuit used to measure the frequency v_i of a pulsed RF signal.

The frequency of the VCO is continuously monitored by a digital frequency counter. The preliminary tests show that the frequency of the VCO is very close to the frequency of the pulsed RF signal. To the limit, when a cw RF signal is applied to the input, then the two frequencies are equal. Thus, the frequency of the RF pulsed signal is measured as frequency of the VCO.

The test circuit was achieved using the specialized integrated circuit 74HCT4046 (dashed frame in Fig. 1 and Fig. 2) which can oscillate up to 19 MHz. This circuit contains the phase comparator and VCO [7]. As an analog switch is used one channel of the integrated circuit 74HCT4051 [8] while the operational amplifier is a MCP601 type. The low pass filter was built using discrete elements.

In order to verify the accuracy of the proposed method preliminary measurements using a known RF oscillation source has been performed. The signal provided by a SRO oscillator is simulated by the circuit shown in Fig. 3. As a RF oscillator was used an external synthesizer which is characterized by a known and very stable output frequency. The cw signal provided by this synthesizer is applied to an input of an analog gate. A low frequency square wave signal which simulates the quenching signal is applied to the other input, acting as a gate signal. The width of the low frequency pulses τ (duty cycle of the gate signal) can be varied. A RF pulsed signal is obtained to the output of the gate.

The frequency of the VCO, v_o , for different values of the duty cycle τ/T has been measured. In the Table 1 ratio $(v_o - v_i)/v_i$ as a function of the duty cycle τ/T of the gate signal is presented. The parameter v_o is frequency of the VCO measured by a digital frequency counter while v_i is frequency of the input signal (reference signal).

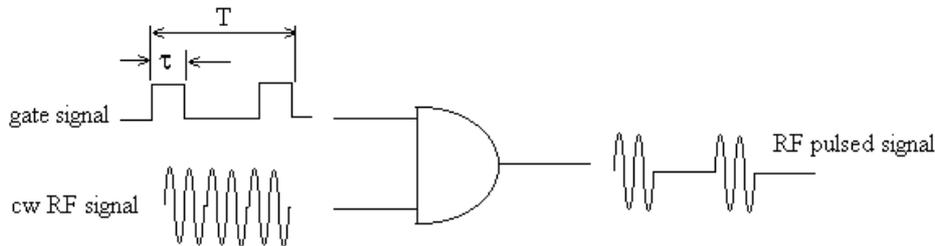


Fig. 3 – Circuit used to obtain a RF pulse signal simulating the SRO signal.

Table 1

Relative error of measured frequency as a function of duty cycle of the gate signal

τ/T	$(\nu_o - \nu_i)/\nu_i$ using modified topology shown in Fig. 2	$(\nu_o - \nu_i)/\nu_i$ using conventional topology shown in Fig. 1
0.02	-0.032	-0.97
0.1	-0.008	-0.897
0.2	-0.004	-0.694
0.3	0.0008	-0.596
0.4	0.0012	-0.486
0.5	0.0002	-0.376
0.6	0.0004	-0.27
0.7	-0.0008	-0.164
0.8	-0.0002	-0.08
0.9	-0.001	-0.022

Experimental measurements have been done at $\nu_i = 5$ MHz while the frequency of the gate signal $1/T = 20$ kHz. For comparison, is also presented the same ratio when the analog switch is disabled *i.e.* the test circuit operates in a conventional topology. The results demonstrate that proposed method is suitable for measuring the frequency of a RF pulsed oscillator.

REFERENCES

1. F. Frink, *The Basic Principles of Superregenerative Reception*, Proc.IRE, **76** (1938).
2. W. E. Bradley, *Superregenerative Detection Theory*, Electronics, **21**, 96 (1948).
3. R. H. Enns, G. C. McGuire, *Nonlinear Physics with Maple for Scientists and Engineers*, Birkhauser, 1997.
4. L. A. Darrell, *A Low Cost Superregenerative SAW Stabilized Receiver*, IEEE Trans. on Consumer Electronics, **CE-33**, 3 (1987).
5. B. Duverneay, C. R. White, E. J. Inigo-Santiago, M. Flynn, *A 1 GHz Superregenerative Receiver*, University of Michigan, College of Engineering, 2003.
6. F. M. Gardner, *Phaselock Techniques*, John Wiley & Sons, Inc, 1967.
7. *** Philips Semiconductor, 74HCT4046 Datasheet, 1997.
8. *** ST2003 STMicroelectronics, 74HCT4051 Datasheet, 2003.