TEMPERATURE INFLUENCE ON THE CAPACITANCE-VOLTAGE HYSTERESIS OF TRANSPARENT a-IGZO/PZT/FTO MFS-HETEROSTRUCTURE

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Abstract. Capacitance-voltage (C-V) hysteresis of metal-ferroelectric-semiconductor (MFS) structure based on a-$In_2GaZnO_{5.5}$ and $Pb_{0.2}Zr_{0.8}TiO_3$ layers are recorded in the 350–470 K range. The structure is grown on FTO/glass to obtain a transparent MFS. The memory functionality of the heterostructure is proved through C-V and P-V characteristics. The memory window is dependent on the temperature, the largest value of 2.5 V being obtained at 470 K, where the contribution of the ferroelectric-semiconductor interface defect states is minimized. The direction of C-V hysteresis is clockwise at 350 K, and it turns counterclockwise at higher temperatures where the ferroelectric polarization has the main contribution.

Key words: metal-ferroelectric-semiconductor, a-IGZO, PZT, transparent heterostructure, non-volatile memory.

1. INTRODUCTION

Ferroelectric materials can be used to replace or to be combined with the gate oxide from a thin film field effect transistor (TF-FET), being possible to develop new FETs with memory functionality [1−5]. Thus, electronic non-volatile memory devices can be designed by integrating ferroelectric layers in metal-ferroelectric-semiconductor structures (MFS). The hysteresis acquired on such structures by capacitance − voltage (C-V) measurements should indicate if the channel (semiconductor) conductance can be switched and memorized, while the memory window of the device being the shift in the value of the flat-band voltage when the bias voltage is swept between depletion and accumulation. $Pb(Zr,Ti)O_3$ (PZT) is a very good ferroelectric material, with a high remnant polarization (80–100 $\mu C/cm^2$) [6−9] that can be integrated in devices containing oxides, while its use in matured silicon technology is still under R&D development due to an imperfect interface

with silicon [10−12] issues reported also for other ferroelectric materials with perovskite structure [13, 14]. A reliable semiconductor that has already been used as channel semiconductor in TFTs is amorphous indium gallium zinc oxide (a-IGZO) [15−19]. This material has higher free carrier mobility values in the conduction channel compared to amorphous silicon, being also transparent in the visible region of the electromagnetic spectrum. Heterostructures based on a-IGZO and PZT might exhibit good memory properties as a result of the high polarization in the ferroelectric layer and high mobility of the carriers in the amorphous oxide semiconductor. The interaction between these two materials was presented, to our best knowledge, in only one study performed by Park *et al.* [2], without pointing out the correlation between the ferroelectric properties (polarization) and memory response. The advantage of transparency of these MFS heterostructures should be also considered.

In this paper the temperature dependence of the memory response in a MFS structure based on a-$In_2GaZnO_{5.5}$ as semiconductor channel and $Pb_{0.2}Zr_{0.8}TiO_3$ as gate oxide is reported. The structural and optical properties of the heterostructure are also considered. The entire structure was grown on glass substrate, having a transparent FTO ($F:SnO_2$) bottom electrode.

2. EXPERIMENTAL

2.1. MATERIALS AND DEPOSITION

Metal-ferroelectric-semiconductor and metal-ferroelectric-metal like structures were grown on glass covered with transparent FTO, which will be used as bottom electrode. The FTO/glass substrates were acquired from Solaronix. The ferroelectric $PbZr_{0.2}Ti_{0.8}O_3$ was synthesized using a sol-gel technique employing alcoxide precursors dissolved in 2-methoxyethanol (Sigma-Aldrich): lead acetate $Pb(CH_3COO)_2 \cdot 3H_2O$ (Aldrich), zirconium propoxide $Zr[O(CH_2)_2CH_3]_4$ (Aldrich) and titanium isopropoxide $Ti[OCH(CH_3)_2]_4$ (Aldrich). The sol-gel PZT layer preparation is already fully presented elsewhere [20, 21]. The semiconductor layer of amorphous IGZO was deposited by RF-magnetron sputtering using an IGZO ceramic target prepared by solid state reaction from starting oxides (In_2O_3, Ga_2O_3 and ZnO) with cation ratio In:Ga:Zn = 2:1:1. The a-IGZO layer was grown at room temperature using a sputtering power of 100 W in a working pressure of $3 \cdot 10^{-3}$ mbar ensured by a mixture of 14 sccm Ar and 0.5 sccm O_2. After semiconductor deposition, the sample was annealed at 200°C for 1 hour in air (dark). Top gold electrodes with 0.3 mm^2 area and ultrathin titanium adhesion layers were deposited by RF magnetron sputtering through a shadow mask on the semiconductor layer to enclose the MFS structure and on the ferroelectric layer to complete a capacitor

metal-ferroelectric-metal (MFM) structure. The thickness of PZT layer is estimated to 200 nm and the a-IGZO layer to 30 nm.

2.2. CHARACTERIZATION TECHNIQUES

The structural characterization was done by analyzing the data acquired with a X-ray Diffractometer (XRD) – Bruker D8 Advance, with a copper anode as the source and nickel filter to eliminate the Cu-K_β contribution to the detected signal, the incident beam being dichromatic (Cu-$K_{\alpha1}$ = 1.54060 Å and Cu-$K_{\alpha2}$ = 1.544 Å). The XRD measurement was achieved in symmetrical coplanar geometry. Transmittance spectra were acquired by using Woolam Variable Angle Spectroscopic Ellipsometer with a Xe lamp as light source. The surface morphology was analyzed with Ntegra Aura NT-MDT Atomic Force Microscope in contact mode.

The polarization–voltage (P–V) measurements were performed using a TF2000 ferritester system equipped with a FE-Module, the capacitance–voltage (C–V) characteristics were acquired using an Agilent LCR meter equipped with a Janis cryostat. The remnant hysteresis was recorded by using the PUND method (Positive-Up-Negative-Down) [22−24].

3. RESULTS AND DISCUSSIONS

The X-ray diffractogram (Fig. 1) acquired on PZT layer in symmetric scan shows sharp intense diffraction peaks corresponding to tetragonal PbZr$_{0.2}$Ti$_{0.8}$O$_3$, indexed according to ICDD pattern 01-070-4260 [25]. The tetragonality of the PZT perovskite is also fingered by the 001/110, 101/110, 002/200, 201/210, 112/211 double peaks. The other peaks (*) are assigned to the FTO.
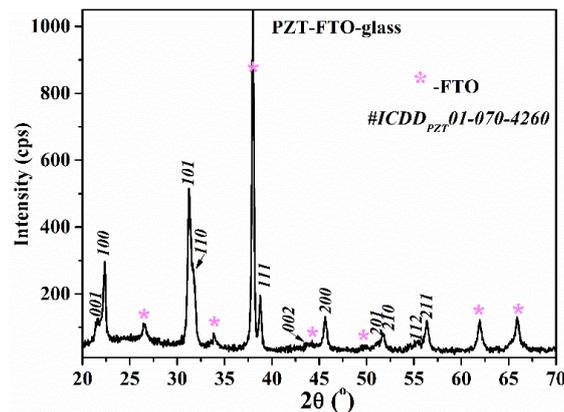

Fig. 1 – XRD θ-θ scan of the PZT/FTO/glass structure.

The surface microstructure of the PZT layer presented in Fig. 2 (5 μm × 5μm) shows a typical island surface for a ferroelectric polycrystalline PZT film [20, 26, 27], with good lateral size uniformity of the grains, with diameters below 100 nm.

The transmittance spectrum of the entire MFS structure (IGZO/PZT/FTO/glass) and the one of solely FTO electrode/glass substrate are presented in Fig. 3. The transparency of the MFS structure in the visible range of the electromagnetic spectrum lies above 65%, while the FTO/glass structure transparency is around 80%.
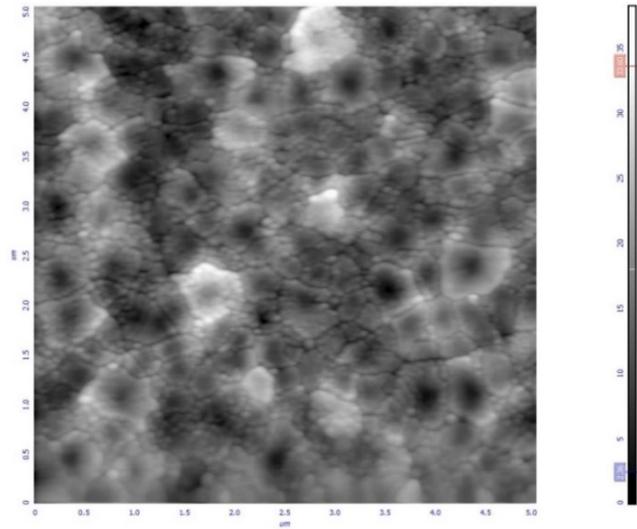

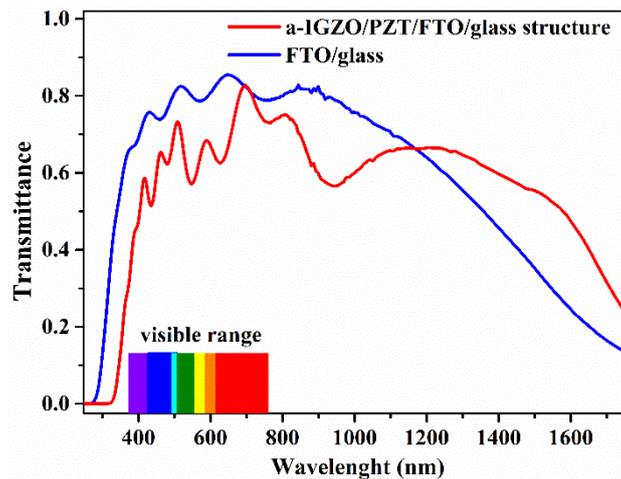Fig. 2 – AFM image of the PZT/FTO/glass structure.

Fig. 3 – Transmittance spectra of a-IGZO/PZT/FTO/glass and FTO/glass.

To analyze the memory response of the a-IGZO/PZT based structure, capacitance-voltage characteristics were acquired at temperatures below Curie temperature of PZT, which is reported to lay between 500 K and 740 K as a function of composition and structure (bulk or thin films with different thicknesses) [28, 29, 30, 31]. The memory functionality is emphasized through the shift of the entire C-V characteristics along the voltage axis as the bias voltage is swept up and down to drive the conduction channel from depletion to accumulation. This shift generates a hysteresis, which orientation depends on the type of conduction in the semiconductor layer, on the amount of the interface states at the semiconductor-ferroelectric interface, and on the presence of the ferroelectric polarization in the PZT layer. Hence, a n-type semiconductor such as IGZO, in combination with a ferroelectric PZT layer, should lead to a counterclockwise C-V hysteresis [7, 32−34] if the effect of the interface states is negligible. However, in the real MFS structures, the C-V hysteresis is a sum result of the hysteresis due to the ferroelectric polarization and the one due to the interface states that are present at the ferroelectric-semiconductor interface. The orientation of the hysteresis produced by the interface states is clockwise. Therefore, if the interface states are in significant amount they can produce a hysteresis dominating the ferroelectric one, leading to an overall clockwise orientation of the hysteresis of the MFS structure.

In Fig. 4 (a–d) are shown the capacitance-voltage dependencies recorded at temperatures from 350 K to 470 K (at 100 kHz). Excepting the C-V characteristic at 350 K that has a clockwise orientation, all the other C-V dependencies show a counterclockwise oriented hysteresis. This behavior suggests a strong influence of the ferroelectric polarization compared to the contribution of electric active defect states at the ferroelectric-semiconductor interface. The C-V hysteresis orientation drastically changes with the temperature, and the memory window enlarges by increasing the temperature. At 400 K the memory window is quite low and the C-V hysteresis is quasi-counterclockwise oriented, which suggests that the interface defect states partially compensate the ferroelectric hysteresis. But when the temperature is increased further, the C-V become completely counterclockwise oriented and the memory response is highly improved, reaching memory window of 2.5 V (values that are higher than those of MFS structures with silicon as channel semiconductor [35−37]). Changing the C-V hysteresis direction and enlarging the memory window by increasing the temperature can be fully explained by the existence of defect states localized at the interface between polycrystalline ferroelectric layer and the amorphous n-type semiconductor. At lower temperatures (≤ 350 K) the recorded clockwise hysteresis is similar with a MOS C-V characteristic. The n-type a-IGZO is in depletion when on the ferroelectric layer is applied a negative voltage, and the capacitance of the entire structure is low. When the polarity on the ferroelectric is reversed, the semiconductor shifts to accumulation and mobile charges are injected at the

interface and some part of these charges will be trapped. When the temperature is low, the trapped carriers are not able to follow the slight variation of voltage induced by the applied *ac* signal, therefore the generated hysteresis might have a clockwise direction if the interface charges will exceed the polarization effect induced by the ferroelectric component (Fig. 4a). When the temperature is higher ($T \geq 400$ K), the trapped interface charges react to the applied voltage and the hysteresis associated to these is diminished, the polarization contribution become more important and the overall hysteresis switches to counterclockwise as it is primary influenced by the ferroelectric polarization [7, 32, 33]. This effect improves more and more as the temperature is increased.
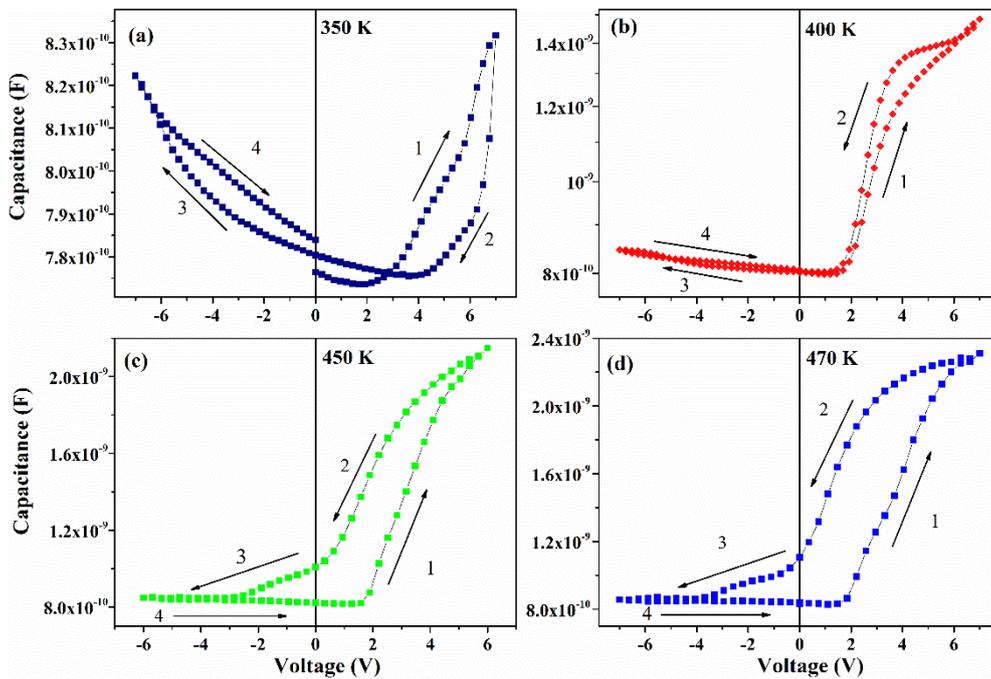

Fig. 4 – Capacitance – voltage characteristics at 350 K (a), 400 K (b), and 450 K (c) and 470 K (d) obtained by measuring the a-IGZO/PZT/FTO/glass MFS structure.

Dynamic and remnant ferroelectric hysteresis measurements were recorded on both MFM and MFS structures. In Fig. 5 are presented the dynamic hysteresis loops in polarization-voltage dependence of capacitor – like Au/PZT/FTO structure (a) and MFS Au/a-IGZO/PZT/FTO (b). The capacitor structure exhibits a well-defined P-V loop that is characteristic to a performant polycrystalline ferroelectric perovskite layer. After integrating the amorphous semiconductor layer, the shape of the hysteresis loop is slightly altered due to supplementary defect states resided at ferroelectric-semiconductor interface and/or in the amorphous semiconductor layer.

These charges delay the reversibility of the polarization and produce supplementary dielectric losses through conduction. It is remarkable the electrical withstand of both MFM and MFS structures, which support voltages up to ± 15 V (3 000 kV/cm).

In order to extract the remnant component of polarization from the overall response of the PZT layer from the MFS structure, a PUND measurement was performed (Fig. 5c). This investigation reveal exclusively the ferroelectric response of the IGZO/PZT based structure, showing a precise memory of the applied field oriented electrical dipoles. The two peaks shown in current-voltage dependence (Fig. 5c) are clear marks of polarization switching.
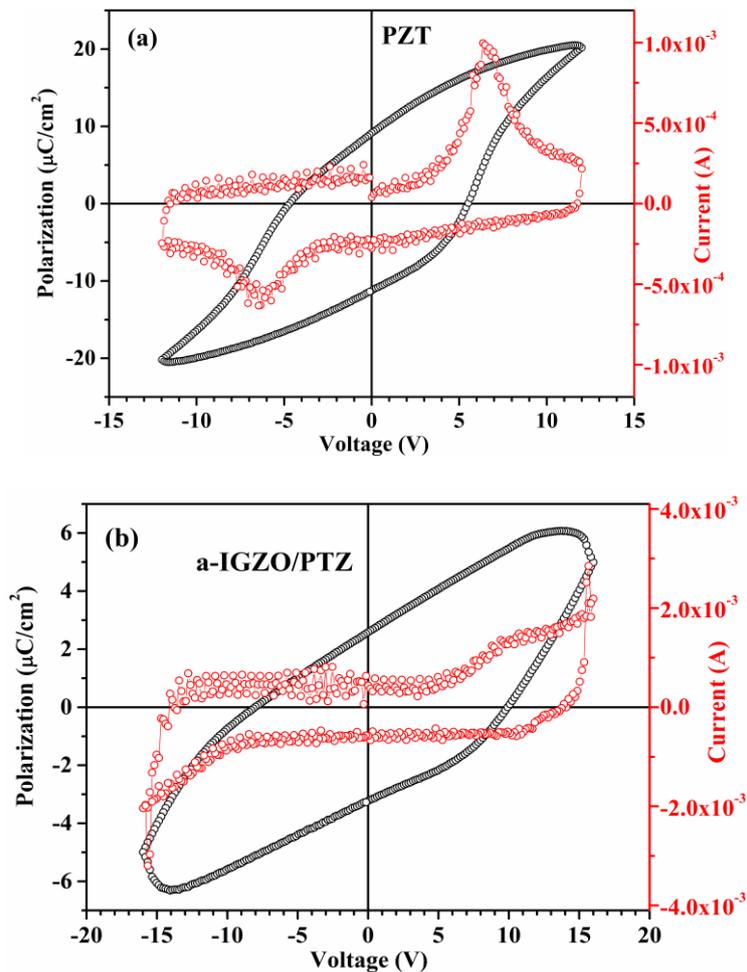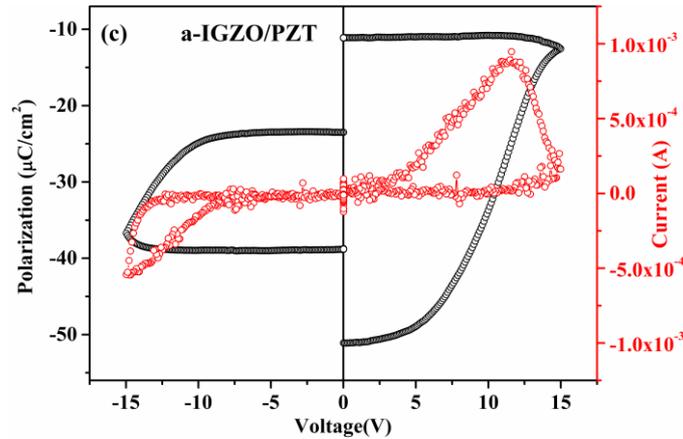

Fig. 5

Fig. 5 (continued) – Dynamic ferroelectric loops measured on MFM (a) and MFS structures (b);
Remnant hysteresis loop measured on MFS structure (c).

4. CONCLUSIONS

Metal-ferroelectric-semiconductor and metal-ferroelectric-metal like transparent structures were grown on FTO/glass substrates, the transparent FTO being used as bottom electrode, $PbZr_{0.2}Ti_{0.8}O_3$ as ferroelectric layer, while in the MSF structure being also integrated the a-IGZO layer. The dependence on temperature of the memory response of the MFS heterostructure was investigated, together with the structural and optical properties of the structure. The ferroelectric properties of both type of structures – parallel plate capacitor MFM and MFS – were investigated by dynamic and remnant P-V hysteresis measurements. The key parameter that influence the memory performance of MFS structure is the temperature, which controls the capacitance-voltage hysteresis direction through the a-IGZO-PZT interface defect states. At lower temperatures (350 K) the C-V hysteresis is clockwise oriented due to the preponderant contribution of the electric active defect states, whereas at higher temperature ($\geq$ 400 K) the main contribution is given by the ferroelectric polarization which induces counterclockwise direction of the C-V hysteresis. The memory window is also temperature dependent, enlarging as the temperature increases. These preliminary results suggest that MFS structures based on a-IGZO-PZT combination can be used for transparent electronics as field effect transistors with memory functionality. Further study are needed in order to elucidate the nature of the interface states at the a-IGZO-PZT interface and to find ways to reduce their influence on the memory properties.

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